



White Rabbit Switch

The **White Rabbit Switch** (WRS) is a central element of White Rabbit networks, enabling ultra-precise time and event distribution. Developed at CERN, it was thoroughly tested under the demanding conditions of the world's largest and most powerful hadron collider infrastructure.

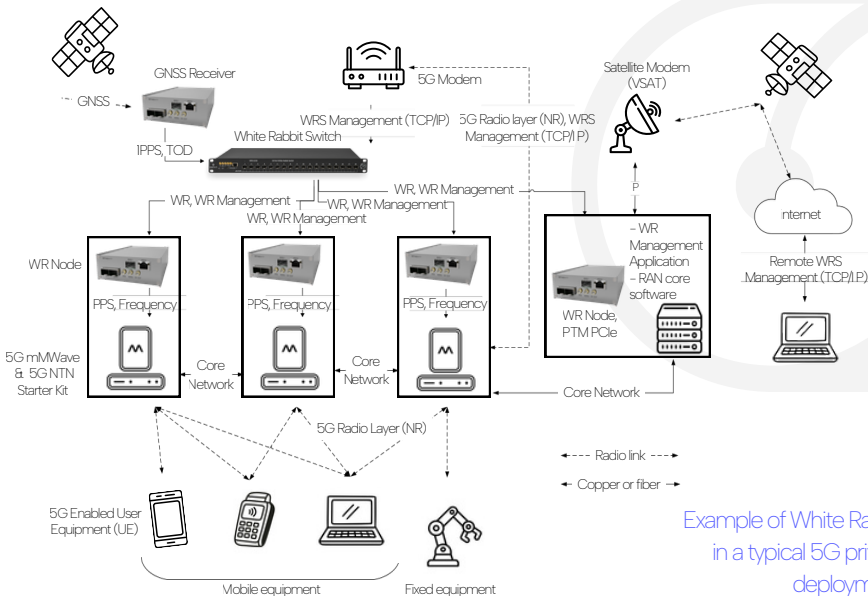
Application possibilities

The main applications of White Rabbit are in control and data-processing systems that require deterministic timing over long distances, in particular:

- Telecommunications (5G)
- Financial transactions (HFT)
- Power grid synchronization
- Geopositioning
- Scientific infrastructures (e.g., particle accelerators, telescope arrays)

As an example of application, we are developing for the European Space Agency (ESA) key components that enable the integration of terrestrial private mmWave 5G networks with satellite-based 5G NTN services.

The project will deliver a 5G mmWave base station prototype with ultra-precise time and frequency synchronization, achieving up to 10 Gbps throughput, low latency, and 5G NTN compatibility. The solution will be commercialized through integration into the product portfolios of Creotech Instruments and Microamp Solutions.



Example of White Rabbit integration
in a typical 5G private network
deployment

Technical Specification

Front Panel

- 5 SMC connectors (1-PPS input and output, 62.5 MHz output, 10 MHz input)
- 18 cages for Gigabit SFP transceivers (connected to Xilinx GTXs)
- 10/100 Ethernet management port (connected to ARM CPU)
- Mini-USB UART management port (connected to ARM CPU)
- Power and Status LEDs
- Link and Act LEDs for each SFP cage

Memory

- 64MB DDR2
- 256MB NAND
- 8MB boot flash

Programmable resources

- Xilinx Virtex-6 FPGA (LX240T FFG1156)
- ARM Atmel AT91SAM9G45 CPU – 400MHz

Clocking resource

- 1x Low-Jitter Clock Generator (Synthesizer 28–683MHz TI CDCM61002, used as DMTD offset clock in WR Switch HDL)
- 1x 25MHz VCXO, FRETHER025 controlled by DAC with SPI interface (AD5662 16bit 2.7–5.54V, used to drive CDCM61002 generator)
- 1x 25MHz VCO controlled by DAC with SPI interface (AD5662 16bit 2.7–5.54V, used to drive AD9516 generator)
- 1x 25MHz XO oscillator FNETHER025 (main FPGA clock)
- PLL – 14 Output Clock Generator with Integrated 1.6 GHz VCO (AD9516, clock signals for Xilinx GTXs, μ TCA connectors)
- 1x Internal Oscillator (VM53S3–25,000, tuned to follow WR master clock or followed in Free Running mode)

Back Panel

- 2x Mini-USB/UART debugging port (connected to ARM CPU and FPGA I/O pins)
- 2x cooling fan
- 2x microswitch, power button
- 1x grounding connector

Software

- Linux – kernel v3.16.38
- Timing – WRP daemon (node discovery, etc.) PTPV2 daemon

Switching

- 1x protocols (multicasting, spanning tree, GMRP/–GARP)
- VLAN Tagging
- SNMP switch management

Other

- Protocols: TCP/IP, SSH, SNMP, TFTP, DHCP, ARP, DNS
- 1x FPGA JTAG connector
- 1x ARM JTAG connector
- 2x I2C multiplexer (PCA9548A)
- 1x I2C GPIO driver (PCA9554PW, driving Power and Status LEDs on the front panel)
- 9x I2C GPIO driver (PCA9554PW, driving LEDs for each SFP cage)
- Power supply 100–240VAC, 2.0A, 50–60Hz input, 12VDC, 6.66A, 80W output

Box dimensions: 19" 1U casing, 447 mm x 44 mm x 223 mm

White Rabbit Switch with Low Jitter Daughterboard

- 10 MHz input clock for GrandMaster operation
 - wide input power range, from –10 dBm to 20 dBm, sinewave or square
- AD9516–4 low noise PLL for clock synthesization
- 16-bit DAC AD5662 to control the oscillator (used by White Rabbit PTP core)

Low jitter VCTCXO, 20MHz:

- Connor–Winfield DOT050 VCTCXO (DOT050V–020.0M)
 - selected as fully protected from airflow
- Option to install another oscillator (14x9mm footprint)
 - Abracom ABLNO VCTCXO
 - Crystek CCHD–950 VCTCXO
 - IQOV–162–3 OCXO (CMOS output)
- Jitter (10 Hz to 100 kHz) < 2 ps RMS (typical 1/5 ps RMS)*

*depending on configuration



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